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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/754,546	01/12/2004	Jae-Bon Koo	61610118US	9275
58027	7590	03/21/2006	EXAMINER	
H.C. PARK & ASSOCIATES, PLC 8500 LEESBURG PIKE SUITE 7500 VIENNA, VA 22182			NGUYEN, THANH NHAN P	
			ART UNIT	PAPER NUMBER
			2871	

DATE MAILED: 03/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

832

Office Action Summary	Application No. 10/754,546	Applicant(s) KOO ET AL.	
	Examiner (Nancy) Thanh-Nhan P. Nguyen	Art Unit 2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01 March 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-13 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-4, 6, 8-13 is/are rejected.
- 7) ☒ Claim(s) 5 and 7 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 16 June 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This communication is responsive to RCE dated 3/1/2006.

Claims 14-15 are canceled; claims 1-13 are pending for the examination.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 10-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Ohtani et al U.S. Patent No. 6,303,963.

Regarding claim 10, Ohtani et al discloses a flat panel display having a matrix-type array of sub-pixels, each of which comprises a driving thin film transistor (3503), a first electrode (3609) driven by the driving thin film transistor, and a second electrode (3613) driving a light emission unit (3505) together with the first electrode, [see fig. 18]; wherein the driving thin film transistor comprises semiconductor channels which are derived from a semiconductor layer, and heterogeneous straight lines are separated from each other on the semiconductor layer, and wherein each of the semiconductor channels comprises at least one of the heterogeneous straight lines, [see figs. 2D, or 6B-6E, or 7A-7D].

Regarding claim 11, inherently, the semiconductor channels comprise the same number of the heterogeneous straight lines.

Regarding claim 12, inherently, the semiconductor channels has a length equal to a value obtained by multiplying the width of a laser beam irradiated for crystallization of amorphous silicon into polycrystalline silicon by the percentage of the area of the semiconductor layer at which overlap of the laser beam does not occur.

Regarding claim 13, Ohtani et al discloses the heterogeneous straight lines are separated from each other by the same distance, [see fig. 7D].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-4, 6, 8 & 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohtani et al in view of Komiya et al U.S. Patent No. 6,456,013.

Regarding claim 1, Ohtani et al discloses a flat panel display having a matrix-type array of sub-pixels, each of which comprises a driving thin film transistor (3503), a first electrode (3609) driven by the driving thin film transistor, and a second electrode (3613) driving a light emission unit (3505) together with the first electrode, [see fig. 18]; wherein the driving thin film transistor comprises semiconductor channels which are derived from a semiconductor layer, and heterogeneous straight lines are separated from each other on the semiconductor layer, wherein at least one of the semiconductor channels comprise at least one of the heterogeneous straight lines, [see figs. 2D, or 6B-6E, or 7A-7D].

Ohtani et al lacks disclosure of an imaginary line connecting the semiconductor channels of one column is not parallel to the heterogeneous straight lines.

Komiya et al discloses an imaginary line connecting the semiconductor channels of one column is not parallel to the heterogeneous straight lines, [see fig. 3], for the benefit of suppressing the leak current in the switching thin film transistors (TFT) to maintain the potential of the gate electrode of the element driving TFT at a fixed level, thereby allowing the electroluminescence (EL) element to emit light at a desired luminance, [see col. 5, lines 4-7]. Therefore, at the time the invention was made, it would have been obvious to one ordinary skill in the art to have an imaginary line connecting the semiconductor channels of one column is not parallel to the heterogeneous straight lines for the benefit of suppressing the leak current in the switching thin film transistors (TFT) to maintain the potential of the gate electrode of the element driving TFT at a fixed level, thereby allowing the electroluminescence (EL) element to emit light at a desired luminance.

Regarding claim 8, Ohtani et al discloses the heterogeneous straight lines are separated from each other by the same distance, [see fig. 7D].

Regarding claims 2-4, 6 & 9, Ohtani et al lacks disclosure of the imaginary line connecting the semiconductor channels of one column is in a non-straight line; the imaginary line connecting the semiconductor channels of one column is a zig-zag line, wherein the zig-zag line has a regular zig-zag pattern; wherein the zig-zag line has a two-step zig-zag pattern; wherein the heterogeneous straight lines are separated from

Art Unit: 2871

each other by the same distance and the width of the zig-zag line is larger than the distance between adjacent two of the heterogeneous straight lines.

However, all the listed features in claims 2-4, 6 & 9 are described in Komiya's disclosure, particularly in fig. 3, as being for the benefit that discussed in claim 1 above.

Allowable Subject Matter

Claims 5 & 7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The claim is allowable over the prior art of record because none of the references, either alone or in combination, discloses or renders obvious the flat panel display comprising the imaginary line connecting the semiconductor channels of one column is a zig-zag line, wherein the zig-zag line has a non-uniform zig-zag pattern, or wherein the zig-zag line has three-step zig-zag pattern.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to (Nancy) Thanh-Nhan P. Nguyen whose telephone number is 571-272-1673. The examiner can normally be reached on M-F/9-5:30.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim can be reached on 571-272-2293. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2871

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

(Nancy) Thanh-Nhan P Nguyen
Examiner
Art Unit 2871
-- March 17, 2006 --

TN


ANDREW SCHECHTER
PRIMARY EXAMINER